CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for testing a plurality of content addressable memory (CAM) cells in a CAM device, comprising the steps of:

(a) testing said CAM device for stuck match lines;

(b) testing said CAM device for weak-pull down lines;

(c) testing each CAM cell in said CAM device to locate a faulty CAM cell; and

(d) for each faulty CAM cell identified in step (c), diagnosing a cause of fault for said faulty CAM cell by applying at least one signal and reading a state of a match line associated with said faulty cell.

2. The method of claim 1, wherein step (c) is performed after both steps (a) and (b), and step (d) is performed after step (c).

3. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a mask value of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

4. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical one;

setting a complement search data line of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

5. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to logical zero.

6. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to logical one.

7. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty search data line if said match line is set to logical one.

8. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty search data line if said match line is set to logical zero.

9. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty complement search data line if said match line is set to a logical one.

10. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty complement search data line if said match line is set to logical zero.

11. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an stuck open fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical one.

12. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an short circuit fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical zero.

13. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying an stuck open fault with a transistor having a gate coupled to a complement of a data storage node if said match line is set to a logical one.

14. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to is set to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a complement of a data storage node, if said match line is set to logical zero.

15. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

16. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

17. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to one.

18. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to logical zero.

19. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one; and

setting a complementary search data line of said faulty CAM cell to a logical zero;

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

20. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

21. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

22. The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

23. A system for testing a CAM device comprising:

an interface for sending and receiving signals from the CAM device; and

a processor, coupled to said interface, for controlling signals that are sent to the CAM device and for reading signals received from the CAM device,

wherein said processor operates said interface to test said CAM device for stuck match lines, weak-pull down lines, and faulty CAM cells; and

wherein for each faulty CAM cell said processor operates said interface to diagnose a cause of fault for each faulty CAM cell by applying at least one signal and reading a state of a match line associated with the faulty CAM cell.

24. The system of claim 23, wherein said processor applying at least one signal by:

setting a mask value of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

25. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical one;

setting a complement search data line of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

26. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to a logical zero.

27. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to logical one.

28. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty search data line if said match line is set to logical one.

29. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty search data line if said match line is set to logical zero.

30. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty complement search data line if said match line is set to a logical one.

31. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty complement search data line if said match line is set to logical zero.

32. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an stuck open fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical one.

33. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an short circuit fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical zero.

34. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying an stuck open fault with a transistor having a gate coupled to a complement of a data storage node if said match line is set to a logical one.

35. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to is set to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a complement of a data storage node, if said match line is set to logical zero.

36. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

37. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

38. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to one.

39. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to logical zero.

40. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

41. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

42. The system of claim 23, wherein said processor applies said at least one signal by::

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

43. The system of claim 23, wherein said processor applies said at least one signal by:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

44. A system for testing a CAM device comprising:

means for testing for stuck match line within the device;

means for testing for weak-pull down lines within the device;

means for identifying faulty CAM cells within the device; and

means for diagnosing faulty CAM cells identified by said identifying means.